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By: Loren D. Pearson Date: 10/9/02

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Horst Belau et al.

Appl. No. : 09/804,323

Filed : March 12, 2001

Title : Printed Circuit Board Configuration with a Multipole Plug-In Connector

Examiner : Kamand Cuneo

Group Art Unit : 2827

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A M E N D M E N T under 37 C.F.R. § 1.116

Hon. Commissioner of Patents and Trademarks
Washington, DC 20231

S i r :

Responsive to the final Office action dated July 10, 2002, kindly amend the above-identified application as follows:

In the Claims:

Claim 1 (amended). A printed circuit board configuration with a multipole plug-in connector, comprising:

a board having at least two layers, each one of said at least two layers having an edge region and a first of said two layers being an outermost layer and a second of said two layers being directly adjacent said outermost layer;

a plurality of signal conductor tracks disposed in said edge region of said outermost layer;

a plurality of plug pins, each one of said plurality of said plug pins fixed to a respective one of said plurality of said signal conductor tracks in a direction parallel to said one of said layers;

a plurality of ground conductor tracks disposed on said outermost layer;

a side-to-side configuration in which said plurality of said signal conductor tracks and said plurality of said ground conductor tracks are alternatingly disposed on said outermost layer, and in which said plurality of said signal conductor tracks run essentially parallel with respect to said plurality of said ground conductor tracks;

at least one filter capacitor connected between a respective one of said plurality of said signal conductor tracks and a

respective one of said plurality of said ground conductor tracks; and

a ground shielding surface disposed on said directly adjacent layer and covering said side-to-side configuration.

Claim 7 (amended). The printed circuit board configuration according to claim 1, wherein:

said at least two layers includes a second outermost board layer remote from said first outermost board layer, said second outermost board layer having an outer edge region; and

said plurality of said signal conductor tracks defines a first plurality of signal conductor tracks, said plurality of said plug pins defines a first plurality of plug pins, said plurality of said ground conductor tracks defines a first plurality of ground conductor tracks, and said side-to-side configuration defines a first side-to-side configuration, the printed circuit board configuration including:

a second plurality of signal conductor tracks disposed in said edge region of said second outermost board layer;

a second plurality of plug pins, each one of said second plurality of said plug pins fixed to a respective one of said

second plurality of said signal conductor tracks in a direction parallel to said second outermost board layer;

a second plurality of ground conductor tracks disposed on said second outermost board layer and assigned to said second plurality of said signal conductor tracks; and

a second side-to-side configuration in which said second plurality of said signal conductor tracks and said second plurality of said ground conductor tracks are alternatingly disposed on said second outermost board layer, and in which said second plurality of said signal conductor tracks run essentially parallel with respect to said second plurality of said ground conductor tracks.

Add the Following Claim:

--8. The printed circuit board configuration according to claim 1, wherein said board has only two layers.--

--9. A printed circuit board configuration with a multipole plug-in connector, comprising:

a board having at least three layers, each one of said at least three layers having an edge region; a first of said at least three layers defines a first outer board layer, a second of said at least three layers defines an inner board layer,

and a third of said at least three layers includes a second outer board layer remote from said first outer board layer;

a plurality of signal conductor tracks disposed in said edge region of one of said layers;

a plurality of plug pins, each one of said plurality of said plug pins fixed to a respective one of said plurality of said signal conductor tracks in a direction parallel to said one of said layers;

a plurality of ground conductor tracks disposed on said one of said layers and assigned to said plurality of said signal conductor tracks;

a side-to-side configuration in which said plurality of said signal conductor tracks and said plurality of said ground conductor tracks are alternatingly disposed on said one of said layers, and in which said plurality of said signal conductor tracks run essentially parallel with respect to said plurality of said ground conductor tracks;

at least one filter capacitor connected between a respective one of said plurality of said signal conductor tracks and a respective one of said plurality of said ground conductor tracks;

a ground shielding surface disposed on an adjacent one of said layers and covering said side-to-side configuration;

said plurality of said signal conductor tracks defining a first plurality of signal conductor tracks, said plurality of said plug pins defining a first plurality of plug pins, said plurality of said ground conductor tracks defining a first plurality of ground conductor tracks, and said side-to-side configuration defining a first side-to-side configuration, the printed circuit board configuration including:

a second plurality of signal conductor tracks disposed in said edge region of said second outer board layer;

a second plurality of plug pins, each one of said second plurality of said plug pins fixed to a respective one of said second plurality of said signal conductor tracks in a direction parallel to said second outer board layer;

a second plurality of ground conductor tracks disposed on said second outer board layer and assigned to said second plurality of said signal conductor tracks; and

a second side-to-side configuration in which said second plurality of said signal conductor tracks and said second plurality of said ground conductor tracks are

alternatingly disposed on said second outer board layer, and in which said second plurality of said signal conductor tracks run essentially parallel with respect to said second plurality of said ground conductor tracks.--

Remarks:

Reconsideration of the application is requested. Claims 1-9 are now in the application. Claims 1 and 7 have been amended. Claims 8 and 9 have been added.

In item 3 of the Office action, the Examiner rejected claims 1-6 as being obvious over Gentry (U.S. 4,644,092), Osifchin et al. (U.S. 3,093,805), and Kobayashi et al. (U.S. 6,040,524) under 35 U.S.C. § 103(a). The rejection has been noted and the claims have been amended in an effort to define more clearly the invention of the instant application.

Before discussing the prior art in detail, a brief review of the invention as claimed is provided. Amended claim 1 calls for, *inter alia*, a printed circuit board configuration having the following features:

> a board having at least two layers, each one of said at least two layers having an edge region and a first of said two layers being an outermost layer and second of said two layers being directly adjacent said outermost layer;
>
> a plurality of signal conductor tracks disposed in said edge region of said outermost layers;
>
> a plurality of plug pins, each one of said plurality of said plug pins fixed to a respective one of said plurality of said signal conductor tracks in a direction parallel to said one of said layers;
>
> a plurality of ground conductor tracks disposed on said outermost layer;

a side-to-side configuration in which said plurality of said signal conductor tracks and said plurality of said ground conductor tracks are alternatingly disposed on said outermost layer, and in which said plurality of said signal conductor tracks run essentially parallel with respect to said plurality of said ground conductor tracks;

at least one filter capacitor connected between a respective one of said plurality of said signal conductor tracks and a respective one of said plurality of said ground conductor tracks; and

a ground shielding surface disposed on said directly adjacent layer and covering said side-to-side configuration. (Emphasis added by Applicants.)

Amended claim 1 clarifies that the signal conductor tracks are located on an outermost board layer, i.e., the first outer board layer. Furthermore, the ground conductors are located parallel on the outermost board layer. Furthermore, the ground shielding surface is not located on any adjacent board layer, but rather on the board layer that is directly adjacent to the outermost board layer. In addition, claim 8 states that board layer that is directly adjacent to the outermost board layer is the second board layer of only two board layers.

Accordingly, amended claim 1 explicitly states that the signal and ground conductor tracks are always located on an outermost board layer and the ground shielding surface is located on the directly adjacent board layer, so that no additional board layer can be located between an outer board layer and the board layer covered with the ground shielding surface.

In contrast to amended claim 1, the reference does not show a printed circuit board configuration as recited in claim 1 of the instant application.

Accordingly, none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Therefore, claim 1 is patentable over the art. Moreover, because all of the dependent claims are ultimately dependent on claim 1, they are believed to be patentable as well.

In item 4 of the Office action, the Examiner objected to claim 7 but indicated that it contained allowable subject matter. Claim 9 is an independent claim representing the originally-submitted, allowed claim 7.

In view of the foregoing, reconsideration and allowance of claims 1-9 are solicited. In the event the Examiner should still find any of the claims to be unpatentable, please telephone counsel so that patentable language can be substituted. In the alternative, the entry of the amendment is requested as it is believed to place the application in better condition for appeal, without requiring extension of the field of search.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicants

LDP:cgm

October 9, 2002

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